

S/N 09/782,743



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PATENT

Hayes

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: Howard E. Rhodes  
Serial No.: 09/782,743  
Filed: February 13, 2001  
Title: DUAL DOPED GATES

Examiner: Long Pham  
Group Art Unit: 2823  
Docket: 303.592US1

**AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111**

Commissioner for Patents  
Washington, D.C. 20231

This paper is in response to the office action mailed on November 18, 2002. Please amend the above-identified patent application as follows.

**IN THE CLAIMS**

1. (Original) A method comprising:  
preparing a substrate; and  
forming one or more dual gate structures in the substrate using only one mask.
2. (Original) The method of claim 1, wherein preparing a substrate comprises:  
forming a sacrificial oxide layer on a semiconductor.
3. (Original) The method of claim 1, wherein preparing a substrate comprises:  
forming a gate oxide layer on a semiconductor; and  
forming a polysilicon layer on the gate oxide layer.
4. (Original) The method of claim 1, wherein forming one or more dual gate structures in the substrate using only one mask comprises:  
forming a first gate structure having a first conductivity in the substrate, the first gate structure being formed using one or more blanket implants; and  
forming a second gate structure having a second conductivity in the substrate, the second conductivity having a different value than the first conductivity and the second gate structure being formed using only one masking operation.

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